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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,807	12/30/2003	Naoki Nishimura	B588-041	2100

26272 7590 11/22/2005

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EXAMINER	
STARK, JARRETT J	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 11/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/748,807	NISHIMURA, NAOKI	
	Examiner	Art Unit	
	Jarrett J. Stark	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *30 December 2003*. and 3/15/04
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 18 - 24 withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 11/01/2005.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

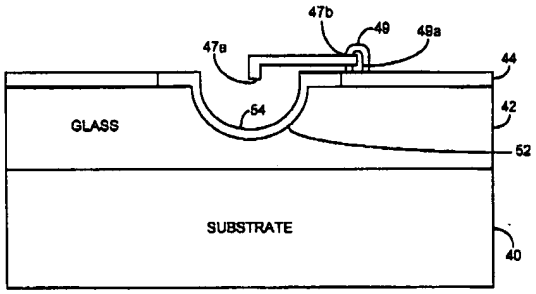
The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

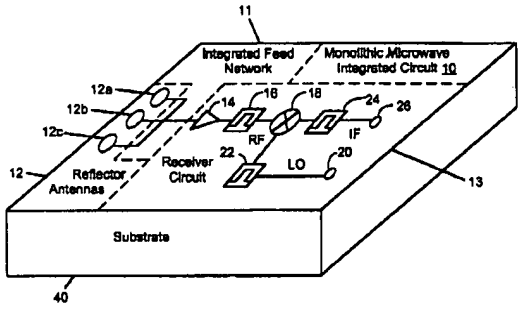
Claim 1, 2, 6 - 8, and 10 - 14 rejected under 35 U.S.C. 103(a) as being unpatentable over Yarbrough et al (US 6,008,776) in view of Yun et al (Thermal and Mechanical Separations of silicon layers from Hydrogen Pattern-Implanted Wafers, Journal of Electronic Materials, Vol. 30, No 8, 2001).

Regarding claim 1, Yarbrough discloses a device which has a semiconductor device (Yarbrough Fig. 1) and a micromachine (Yarbrough Fig. 2E), comprising: a semiconductor layer on which the semiconductor device is formed (Yarbrough Fig. 1); and a substrate on which the micromachine is formed (Yarbrough Fig. 2E), wherein said semiconductor layer and substrate are stacked (Yarbrough Fig. 2E).



REFLECTOR FEED RELEASE AND POSITIONING

FIG. 2e



MEMS INTEGRATED RECEIVER

FIG. 1

Yarbrough does not teach where said semiconductor layer is obtained by separating, at a separation layer, a member which has the separation layer under said semiconductor layer.

Yun teaches the methods of both thermal and mechanical separation of silicon layers for integration of electronic, optical, and micro-mechanical devices (Yun, Intrduction, Lines 1-2).

Therefore it would be obvious to one of ordinary skill in the art to obtain a semiconductor layer by separating, at a separation layer, a member which has the separation layer under said semiconductor layer. Three-dimensional integration of electronic, optical, and micro-mechanical devices will provide for applications in high performance compact microelectronics. As a promising technique for these applications, the ion-cut silicon layer transfer process using hydrogen implantation and wafer bonding was introduced.1,2 (Yun, Intrduction)

Regarding claim 2 , Yarbrough in view of Yun disclose a device which has a semiconductor device and a micromachine, comprising: a semiconductor layer on which the semiconductor device is formed; and a substrate on which the micromachine is formed (Yarbrough Fig. 2E), wherein said semiconductor layer has a first surface and a second surface, the first surface is bonded to said substrate directly or through a bonding layer(Yarbrough Fig. 2E), and the second surface adjoins a layer whose structure is more fragile than said semiconductor layer.

Pertaining to "a layer whose structure is more fragile than said semiconductor layer". Reading just the claim it is unclear what is exactly meant by "more fragile". The fragility can be interoperated from either from a more fragile material or from the thinning process taught in the specification. From the teachings of the references it

would be obvious to one of ordinary skill in the art that a thinned substrate is more fragile than an un-thinned substrate, which is the reason for using a carrier or handle wafer during and after thinning.

Regarding claim 6, Yarbrough in view of Yun disclose the device according to claim 2, wherein the bonding layer includes one of an adhesive and an adhesion layer. (Yarbrough, column 2, line 61) & (Yarbrough Figs. 2E)

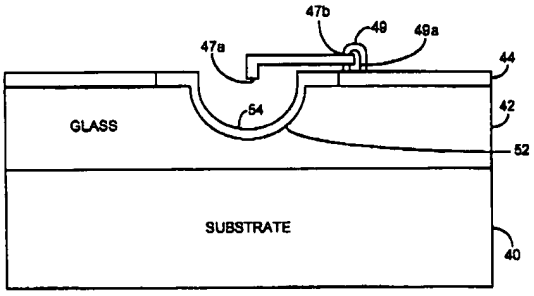
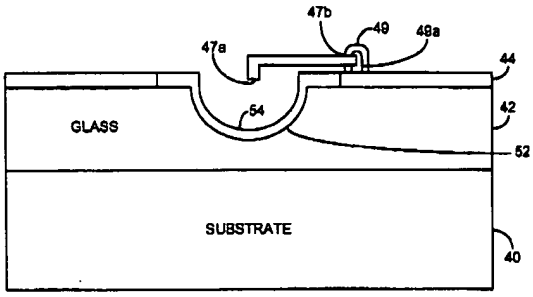


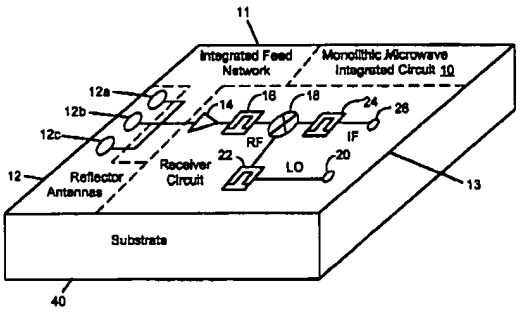
FIG. 2e

Regarding claim 7, Yarbrough in view of Yun disclose a device which has a semiconductor device and a micromachine, comprising: a semiconductor layer on which the semiconductor device is formed; and 20 a substrate on which the micromachine is formed, wherein said semiconductor layer and substrate are stacked (Yarbrough Figs. 1 and 2E), and said semiconductor layer has a thickness of not more than 50 μm. (Yun, page 962, colum 1, line 12 -- Average separation layer was 1.5 μm).



REFLECTOR FEED RELEASE AND POSITIONING

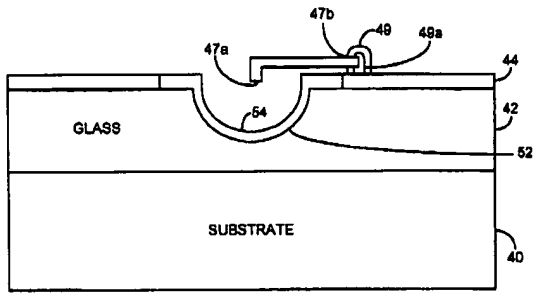
FIG. 2e



MEMS INTEGRATED RECEIVER

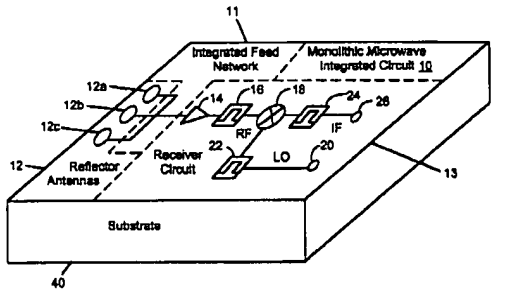
FIG. 1

Regarding claim 8, Yarbrough in view of Yun disclose a device which has a semiconductor device and a micromachine, comprising: a semiconductor layer on which the semiconductor device is formed; and a substrate on which the micromachine is formed, wherein said semiconductor layer and substrate are stacked, and said semiconductor layer has a thickness of not more than 30 μm. (Yun, page 962, colum 1, line 12 -- Average separation layer was 1.5 μm).



REFLECTOR FEED RELEASE AND POSITIONING

FIG. 2e



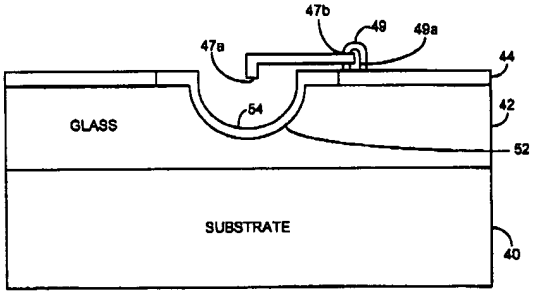
MEMS INTEGRATED RECEIVER

FIG. 1

Regarding claim 10, Yarbrough in view of Yun disclose the device according to claim 1, wherein a semiconductor circuit is formed on said semiconductor layer

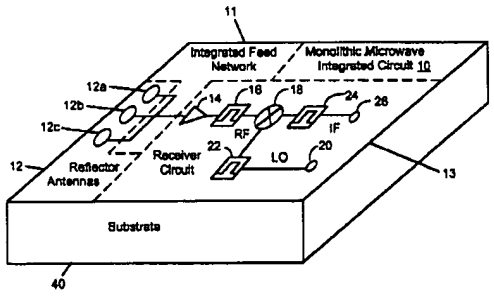
(Yarbrough Figs. 2E), and the semiconductor circuit and micromachine comprise at least part of a radio communication device (Yarbrough,column 1, lines 20-31).

Regarding claim 11, Yarbrough in view of Yun disclose a substrate comprising: a semiconductor layer on which a circuit is formed; and an antenna substrate on which antennas are formed, wherein said semiconductor layer and antenna substrate are bonded together (Yarbrough Figs. 2E), and said semiconductor layer is formed by separating, at a separation layer, a substrate which includes the separation layer(Yun, Intrduction, Lines 1-2)..



REFLECTOR FEED RELEASE AND POSITIONING

FIG. 2e



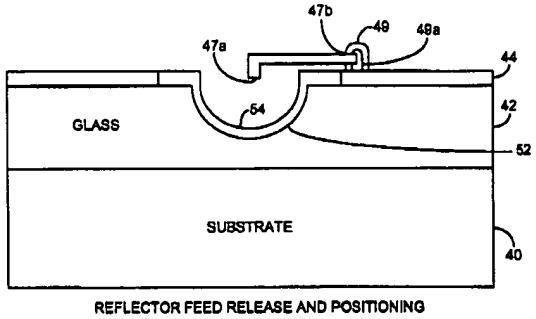
MEMS INTEGRATED RECEIVER

FIG. 1

Regarding claim 12, Yarbrough in view of Yun disclose the substrate according to claim 11, wherein said semiconductor layer has a film thickness of not more than 50 μm. (Yun, page 962, colum 1, line 12 -- Average separation layer was 1.5 μm).

Regarding claim 13, Yarbrough in view of Yun disclose the substrate according to claim 11, wherein said 25 semiconductor layer has a film thickness of not more than 30 It m. (Yun, page 962, colum 1, line 12 -- Average separation layer was 1.5 μm).

Regarding claim 14, Yarbrough in view of Yun disclose the substrate according to claim 11, further comprising a bonding layer which bonds together said semiconductor layer and antenna substrate. (Yarbrough, column 2, line 61) & (Yarbrough Figs. 2E)



REFLECTOR FEED RELEASE AND POSITIONING

FIG. 2e

Claim 3, 4, 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yarbrough et al (US 6,008,776) in view of Yun et al (Thermal and Mechanical Separations of silicon layers from Hydrogen Pattern-Implanted Wafers, Journal of Electronic Materials, Vol. 30, No 8, 2001) in further view of Ito (US 6,566,255).

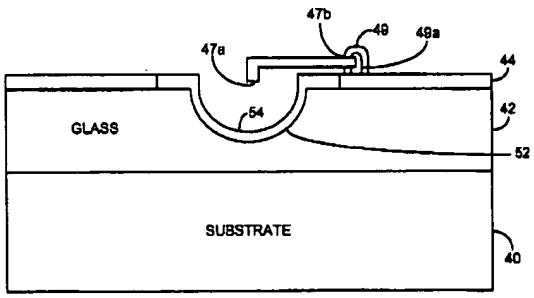
Regarding claim 3 , Yarbrough in view of Yun disclose the device according to claim 2, wherein the layer having the fragile structure includes one of a porous layer and an ion-implanted layer (Yun Fig 1, label - hydrogen peak).

Yun does not specifically disclose the presence of a porous layer.

Ito teaches discloses the presence of a porous layer when forming a separation layer. (Ito, column 5, lines 49-61)

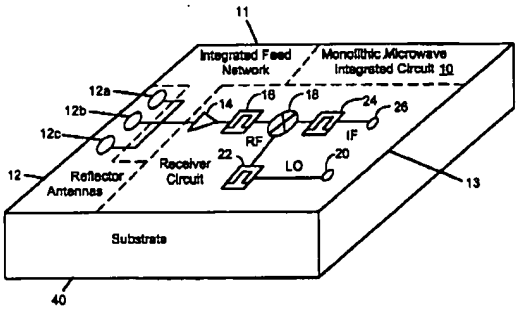
Therefore teachings of the references it is obvious to one of ordinary skill in the art to know that there is a porous layer. An SOI may be an intermediate product or a finished product formed by a SIMOX or bonding method. Especially, the present invention can be preferably applied to an SOI obtained by forming a porous layer on a donor wafer, epitaxially growing a non-porous single-crystal semiconductor layer on the porous layer, bonding the resultant structure to a handle wafer, and then separating the bonded substrate stack at the porous layer, or an SOI obtained by implanting ions of hydrogen or the like into a donor wafer, bonding the donor wafer to a handle wafer, and then separating the bonded substrate stack at a relatively heavily ion-implanted layer. A method for producing an SOI using a hydrogen implantation technique is called Smart Cut_. (Ito, column 5, lines 49-61)

Regarding claim 4 , Yarbrough in view of Yun in further view of Ito disclose a device which has a semiconductor device and a micromachine (Yarbrough Figs. 1 and 2E), comprising: a semiconductor layer on which the semiconductor device is formed; and a substrate on which the micromachine is formed, wherein said semiconductor layer and substrate are stacked, and said semiconductor layer is formed by epitaxial growth. (Ito, column 5, line 53)



REFLECTOR FEED RELEASE AND POSITIONING

FIG. 2e



MEMS INTEGRATED RECEIVER

FIG. 1

Regarding claim 5, Yarbrough in view of Yun in further view of Ito disclose a the device according to claim 4, wherein said semiconductor layer has a first surface and a second surface (Yarbrough Figs. 1 and 2E), the first surface is bonded to said substrate directly or through a bonding layer (Yarbrough Figs. 2E),, and the second surface is bonded to an insulator directly or through a bonding layer, or adjoins the insulator (Yarbrough Figs. 1 and 2E, elements 40 and 42),.

Claim 9 is rejected under 35 U.S.C. 102(b) as being anticipated by Yarbrough et al (US 6,008,776) in view of Yun et al (Thermal and Mechanical Separations of silicon layers from Hydrogen Pattern-Implanted Wafers, Journal of Electronic Materials, Vol. 30, No 8, 2001) in further view of Livingston et al. (US 6,388,631).

Regarding claim 9, Yarbrough in view of Yun disclose the device according to claim 1. Yarbrough teaches in column 1, lines 20-31 the mems device can be made up of a multitude of devices.

Yarbrough does not, however, teach specifically wherein the micromachine includes at least one of a switch, a variable condenser, and an inductor.

Livingston discloses a mems device that is a switch in Figuer 7B.

Therefore it would be obvious to one of ordinary skill in the art to make a device wherein the micromachine includes at least one of a switch, a variable condenser, and an inductor. The cantilevered structure caries the RF contact that provides for metal to metal contact between the input RF line and the output RF line. (Livingston, column 10, lines36-38)

Claims 16 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yarbrough et al (US 6,008,776) in view of Yun et al (Thermal and Mechanical Separations of silicon layers from Hydrogen Pattern-Implanted Wafers, Journal of Electronic Materials, Vol. 30, No 8, 2001) in further view of Gilbert (US 6,396,450).

Regarding claims 16 and 17, Yarbrough et al in view of Yun disclose the substrate according to claim 11.

They do not disclose wherein the antennas are spiral antenna coils.

Gilbert teaches the use of a spiral antenna with a mems switch.

Therefore it would be obvious to one of ordinary skill in the art to use a mems switch along with a spiral antenna. A spiral antenna is typical of such a wideband antenna element. Such elements may be well suited for a single element application, but they cannot be physically placed in a periodic array configuration without overlapping, whereby the spacing between the centroids of the elements is around .lambda./2, where .lambda. is the wavelength of the highest intended frequency of operation.... antenna elements having a virtually unlimited variety of shapes and/or sizes can be formed on the CRT face. Coupling this technology with MEMS switches or similar technology can produce a reconfigurable antenna system having an unparalleled range of flexibility.

Regarding claim 17, Yarbrough et al in view of Yun in further view of Gilbert disclose the substrate according to claim 11, wherein the circuit is electrically connected to the antennas and uses the antennas to transmit and receive radio waves (Gilbert column, 2 lines 46-53).

Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yarbrough et al (US 6,008,776) in view of Yun et al (Thermal and Mechanical Separations of silicon layers from Hydrogen Pattern-Implanted Wafers, Journal of

Electronic Materials, Vol. 30, No 8, 2001) in further view of Tanielian et al (US 6,134,485).

Regarding claim 15, Yarbrough in view of Yun disclose the substrate according to claim 14.

Yarbrough in view of Yun does not teach wherein said bonding layer is an adhesive (Tanielian column 5, lines 58).

Tanielian teaches wherein said bonding layer is an adhesive.

Therefore it would be obvious to one of ordinary skill in the art to bond the two substrates with an adhesive/epoxy layer. The bottom portion 52 of the MEMS 46 includes a cavity 56 defined within a reference support 58. The reference support 58 is designed to allow flip chip bonding of the MEMS 46 to the module substrate 40 of the module 22. The MEMS 46 is mounted to the module 22 using solder bumps or conductive epoxy. The use of flip chip bonding keeps the profile of the module-mounted MEMS 46 to about 0.41 mm (0.016 inches) thick. The reference support 58 advantageously provides feedthroughs so that electrical connections can be made from the backside of the MEMS 46. (Tanielian column 5, lines 53-67)

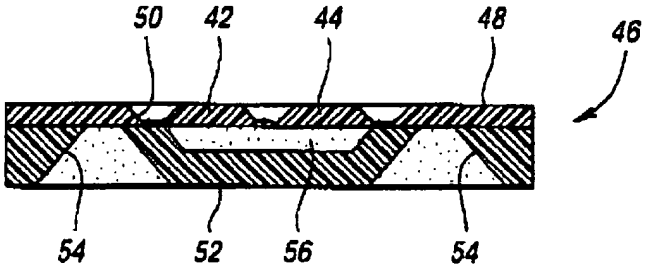


Fig. 7

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jarrett J. Stark whose telephone number is (571) 272-6005. The examiner can normally be reached on Monday - Thursday 6:30AM - 5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571)272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JJS
November 14, 2005

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SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800